IN THE CLAIMS:

Please amend claims 18-35 as follows:

- 1-17. (cancelled)
- 18. (currently amended) A semiconductor device comprising:
 - a semiconductor substrate;
- a first intermediate wiring layer having a first thickness and provided above the semiconductor substrate; and
- a second intermediate wiring layer having a second thickness thinner than the first thickness and provided above the first intermediate wiring layer.
- 19. (currently amended) A semiconductor device according to claim 18, further comprising:
- a lowermost <u>wiring</u> layer nearest to the semiconductor substrate and provided below the first <u>intermediate</u> <u>wiring</u> layer; and
- an uppermost <u>wiring</u> layer farthest from the semiconductor substrate and provided above the second <u>intermediate</u> wiring layer.
- 20. (currently amended) A semiconductor device according to claim 19, wherein a wiring pitch of the first intermediate wiring layer is greater than that of the second intermediate wiring layer.
- 21. (currently amended) A semiconductor device according to claim 19, wherein the first intermediate wiring layer is a layer on which a power source line is formed.

22. (currently amended) A semiconductor device according to claim 19, wherein the first intermediate wiring layer comprises a first area having signal lines and a second area having power source lines, and a pitch of the power source lines is greater than that of the signal lines.

- 23. (currently amended) A semiconductor device according to claim 19, wherein the first intermediate wiring layer comprises a first area having signal lines and a second area having power source lines, and a width of each of the power sources lines is greater than that of the signal lines.
- 24. (currently amended) A semiconductor device according to claim 19, wherein the first intermediate wiring layer is substantially as thick as the uppermost wiring layer.
- 25. (currently amended) A semiconductor device according to claim 19, wherein the second intermediate wiring layer is substantially as thick as the lowermost wiring layer.
- 26. (currently amended) A semiconductor device according to claim 19, wherein all of the uppermost <u>wiring</u> layer, the lowermost <u>wiring</u> layer and the first and second <u>intermediate</u> wiring layers are metal layers.
 - 27. (currently amended) A semiconductor device comprising:

a semiconductor substrate;

an IP core area on the semiconductor substrate;

a peripheral area on the semiconductor substrate except for the IP core area; a first intermediate wiring layer having a first thickness and provided above the

a second intermediate wiring layer having a second thickness smaller than the first thickness and provided above the first intermediate wiring layer in the IP core area.

28. (currently amended) A semiconductor device according to claim 27, further comprising:

semiconductor substrate in the IP core area; and

a lowermost <u>wiring</u> layer nearest to the semiconductor substrate and provided below the first <u>intermediate</u> <u>wiring</u> layer; and

an uppermost <u>wiring</u> layer farthest from the semiconductor substrate and provided above the second <u>intermediate</u> <u>wiring</u> layer.

- 29. (currently amended) A semiconductor device according to claim 28, wherein the first intermediate wiring layer is a layer on which a core power source line is formed.
- 30. (currently amended) A semiconductor device according to claim 28, wherein a wiring pitch of the first intermediate wiring layer is greater than that of the second intermediate wiring layer.
- 31. (currently amended) A semiconductor device according to claim 28, wherein the first intermediate wiring layer is substantially as thick as the uppermost wiring layer.

32. (currently amended) A semiconductor device according to claim 28, wherein the second intermediate wiring layer is substantially as thick as the lowermost wiring layer.

- 33. (currently amended) A semiconductor device according to claim 28, wherein the first intermediate wiring layer comprises a first area having signal lines and a second area having power source lines, and a pitch of the power source lines is greater than that of the signal lines.
- 34. (currently amended) A semiconductor device according to claim 28, wherein the first intermediate wiring layer comprises a first area having signal lines and a second area having power source lines, and a width of each of the power source lines is greater than that of the signal lines.
- 35. (currently amended) A semiconductor device according to claim 28, wherein all of the uppermost <u>wiring</u> layer, the lowermost <u>wiring</u> layer and the first and second <u>intermediate</u> wiring layers are metal layers.